

# High Trap Densities in Wafers from Regions of Reduced Lifetime in Multicrystalline Silicon Blocks

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**Abstract:** Evaluation of bulk material quality through lifetime measurements on as-cut wafers is restricted to material of very poor quality, due to the very high surface recombination velocity of unpassivated wafers. However, we find that the density of non-recombinative traps as extracted from QssPC lifetime measurements on as-cut wafers using the Hornbeck-Haynes trapping model may provide indication on regions of poor material quality, and may as such be employed as a useful tool during wafer inspection. We find that wafers originating from regions in a block corresponding to lifetime dips in the block scan exhibit distinctly higher densities of non-recombinative traps, and that solar cells processed from neighboring wafers reveal a corresponding drop in cell efficiency.

**Key Words:** Multicrystalline Silicon, Recombination Lifetime, Trap Density, Silicon Solar Cells.

## 1 Introduction

Upon directional solidification of multicrystalline silicon (mc-Si) ingots, non-optimum processing can cause certain regions of the ingot to exhibit poor material quality. Prior to wafer cutting, mc-Si blocks (often also referred to as bricks or columns) are therefore routinely investigated by minority carrier lifetime measurements. Regions of poor material quality are commonly identified by the existence of lifetime dips in different regions of the block. Depending on the selection criteria of the wafer producer, blocks exhibiting such lifetime dips can then be chosen as not suitable for further processing, and may be recycled or thrown away. Often, however, only certain regions in the block exhibit poor material quality, whereas the remaining material can be acceptable. It can therefore be preferable to slice wafers from the entire block height, and to distinguish wafers from the bad regions during subsequent wafer inspection. This can reduce production costs, as the need for rejecting the entire block may be eliminated. In this work, we show that quasi-steady-state photoconductance (QssPC) measurements can be used on unpassivated as-cut wafers to identify regions of poor material quality. As the technique is fast, non-destructive, and contact-less, it can easily be implemented in a wafer inspection line.

## 2 Experimental Details

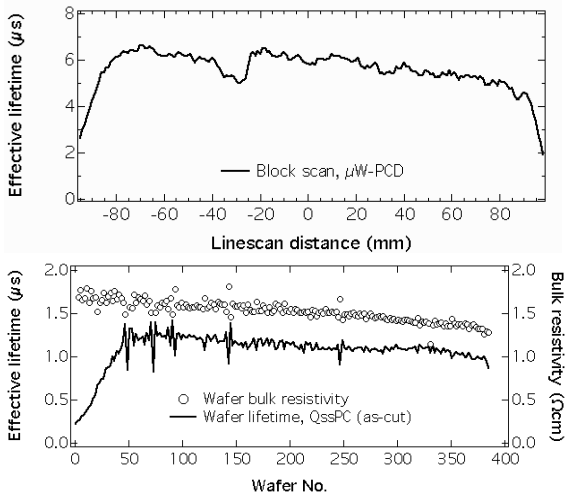
A ~1Ωcm B doped mc-Si ingot was produced in an industrial directional solidification furnace at ScanWafer AS (Norway). The ingot was cut into 25 blocks, each with a base area of 12.5×12.5cm<sup>2</sup>, and the center block was selected for further investigations. Along each of the four vertical sides of the block, nine linescans were performed using a microwave photoconductance decay (μW-PCD) block scanner to investigate the material quality along the block height. From the selected block, only the uppermost 10mm was removed due to the high C concentrations typically experienced in this region of an ingot. Following this, 325μm thick wafers were sliced from the selected block by wire sawing and subsequently cleaned to remove particles and slurry remaining on the surfaces. Then, every second wafer was selected for further processing into solar cells, using a standard industrial process including POCl<sub>3</sub> emitter diffusion, PECVD silicon nitride and screen-printed front and back con-

tacts. The remaining unprocessed wafers were investigated by QssPC without any means of surface passivation [1]. The QssPC apparatus used was equipped with a coil diameter of 8cm, thus effectively measuring an average of mostly the whole wafer area. In mc-Si material, non-recombinative trapping is often significant, causing anomalously high effective lifetimes to be measured by QssPC in low injection [2]. By accommodating for this trapping effect when modeling the QssPC data, additional information related to the density of non-recombinative traps can be extracted. This has been achieved by employing the Hornbeck-Haynes trapping model to fit the experimentally measured data [3].

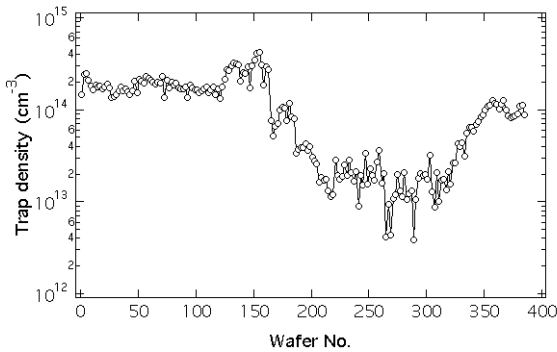
## 3 Results and Discussion

The upper part of Fig.1 shows the average lifetime scan from the bottom to the top (from left to right in the figure) of the mc-Si block. In addition to the low lifetime generally found in the very bottom and top of the block, the block scan reveals a distinct lifetime dip around one third of the block height from the bottom. In many cases, such a block may be rejected from further processing, causing productivity losses for the wafer producer. Alternatively, the block may be cut into sections with removal of the regions corresponding to the low lifetimes. Neither of these procedures are optimal, thus it may be preferable to process wafers from the entire block, and distinguish or reject wafers originating from the region corresponding to the lifetime dip during wafer inspection.

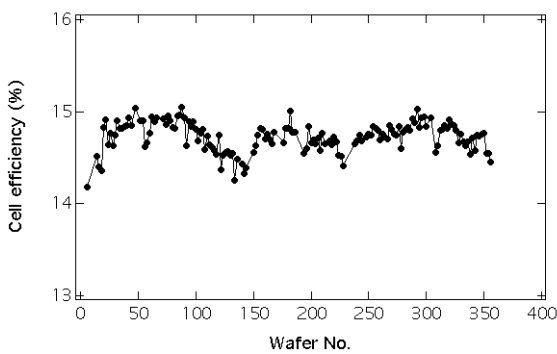
The lower part of Fig.1 shows the effective recombination lifetime as extracted from QssPC measurements on as-cut wafers using the Hornbeck-Haynes analysis, versus wafer number from the bottom of the block. Since as-cut wafers suffer from a very high surface recombination velocity, only wafers with a very low bulk lifetime can be distinguished without employment of any surface passivation treatments. As the figure reveals, wafers from the very bottom of the block is easily distinguished from such lifetime measurements, due to the very low bulk lifetime in this region. However, the wafers originating from the region corresponding to the lifetime dip around one third of the block height are not easily separated from the effective wafer lifetime.



**Fig.1** Block scan average of a mc-Si block (top). Bulk resistivity and effective recombination lifetime in as-cut wafers from different positions within the block (bottom)



**Fig.2** Average density of non-recombinative traps in as-cut wafers from different positions within the block



**Fig.3** Efficiency of solar cells processed on wafers from different positions within the block

Employing the Hornbeck-Haynes analysis on effective lifetimes as measured by QssPC, the density of non-recombinative traps can also be extracted. In Fig.2, the trap density as obtained from lifetime measurements on as-cut wafers is shown versus wafer number from the bottom of the block. As seen in the figure, the trap density is relatively high in wafers originating both from the lower and the upper regions of the ingot. This is typical for mc-Si wafers produced by directional solidification, attrib-

uted mainly to increased concentrations of mobile impurities, e.g. transition metals, towards the bottom and top of such ingots [4].

Interestingly, Fig.2 also reveals that a distinct and well-defined peak in the trap density is exhibited in wafers originating from the region in the block where there is a dip in the lifetime as seen in Fig.1, i.e. centered around wafer number 140. Although there are few precise identifications of the physical origin of non-recombinative trapping, the presence of dislocations or impurity-boron pairs have both been correlated to high trap densities [5]. From the wafer resistivity as shown in Fig.1, no evidence of an increased B concentration near the lifetime dip can be found. However, we have identified the presence of SiC and Si<sub>3</sub>N<sub>4</sub> inclusions in this region. During solidification, C and N segregate towards the melt, causing accumulation at the solidification front. At a critical concentration constitutional super-cooling can occur, leading to incorporation of SiC and Si<sub>3</sub>N<sub>4</sub> inclusions. The higher trap density exhibited in this region could thus emanate from these inclusions themselves, from other impurities precipitated at nucleation sites created by the inclusions, or possibly from dislocations generated around the inclusions.

Every second wafer cut from the block was processed into industrial screen-printed solar cells. In Fig.3, the efficiency of these solar cells is shown versus the corresponding wafer number from the bottom of the block. By comparing the solar cell efficiency with the block scan lifetime in Fig.1, it is readily seen that solar cells processed on wafers originating from the region showing a lifetime dip exhibits a drop in the cell efficiency. Furthermore, solar cells from the very bottom of the block where the as-cut measured effective wafer lifetime is poor, also exhibit reduced cell efficiencies. From the good correspondence between increased trap density, reduced block lifetime, and cell efficiency, it is suggested that extraction of the trap density from lifetime measurements on as-cut wafers may be used as an additional criteria for distinguishing wafers originating from regions of poor material quality in the block.

## 4 Conclusions

We have found that QssPC measurements on as-cut wafers may be used as a tool for sorting wafers from regions of poor material quality in a mc-Si block. By extracting the density of non-recombinative traps, wafers originating from regions where there is a lifetime dip in the block scan can be distinguished, even when the high surface recombination velocity of as-cut wafers prevents detection solely based on the effective wafer lifetime.

## References

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